# Modeling and Validation of a Silicon-Carbide Power Module

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# Abstract


- SiC power modules are gaining popularity for EV traction inverters thanks to higher efficiency and power density.
- The fast-switching characteristics of SiC MOSFETs present challenges in the design and mass production of power modules.
- The study is based on onsemi‘s SSDC SiC power module for EV traction inverters
- This paper explores the impact of package parasitic mismatch and die-level mismatch on the robustness of SiC power modules, using commercially available simulation tools such as ANSYS® Q3D Extractor®, ANSYS® Icepak® and SIMetrix technology.
- The modeling approach is validated with actual test results, followed by an investigation of die level current-sharing.
- We conclude with proposed mitigation measures to enhance the power module's ruggedness.

# Design Challenges

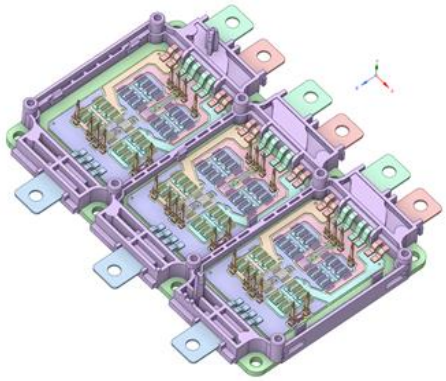
Fast-switching and high-power density of SiC present design challenges:

- More sensitive to package parasitic RLC
- Package layout mismatch induces current-sharing mismatch.
- Die-to-die process variation induces current-sharing mismatch.
- Joule heating of metal interconnect needs to be evaluated in conjunction with CFD simulation to accurately predict temperature profile.

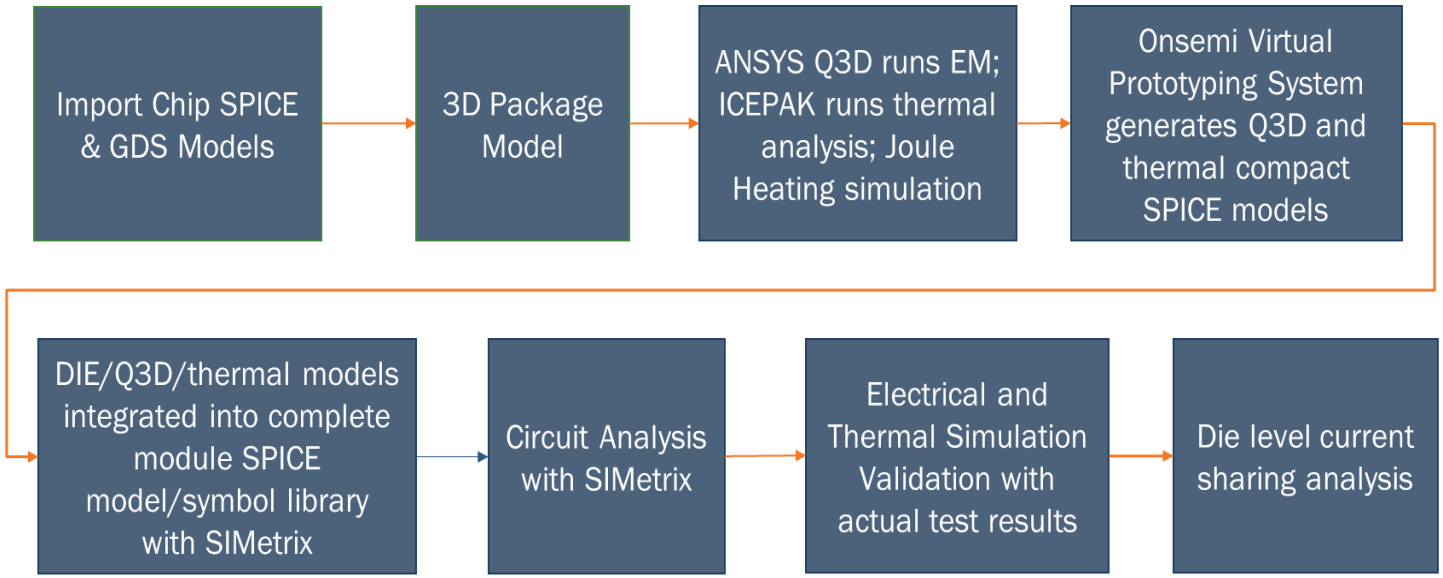
Power module designers are challenged to mitigate risk with proven techniques.

# Modelling and Verification workflow

- Commercially available CAD software and internally developed scripting are utilized to streamline the simulation process
- Electrical and thermal simulation results are validated with actual test results
- Die level current sharing is investigated
- Measures for improving module ruggedness are proposed

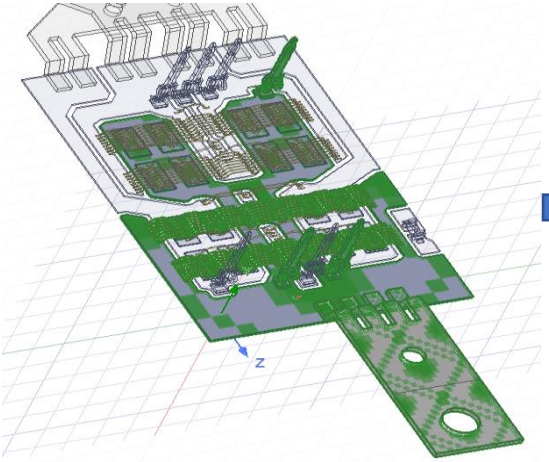


onsemi SSDC SiC 900V power module for EV traction inverter



# Electrical Simulation

- Package RLC equivalent circuit combined with MOSFET SPICE model to form compact model
- Complete circuit assembled to mimic real-world application

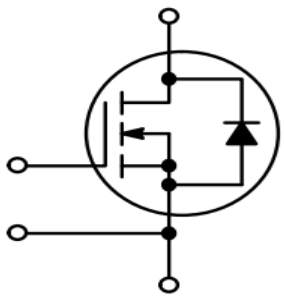


Package RLC extraction

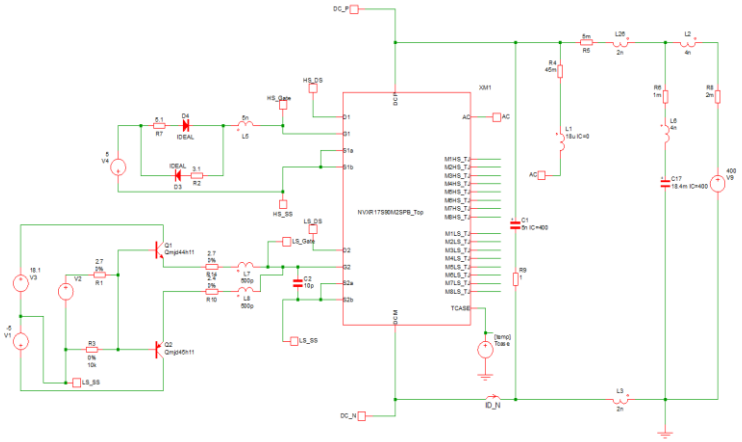
```
.subckt SSDC_900V_SiC_q3d2 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24
+ 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50
+ 51 52 53 54 55 56 57 58 59
XZhalf1 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27
+ 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53
+ 54 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127
+ 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146
+ 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 SSDC_900V_SiC_q3d2_half
XY1 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126 127
+ 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145 146
+ 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162
+ SSDC_900V_SiC_q3d2_parlel
XZhalf2 109 110 111 112 113 114 115 116 117 118 119 120 121 122 123 124 125 126
+ 127 128 129 130 131 132 133 134 135 136 137 138 139 140 141 142 143 144 145
+ 146 147 148 149 150 151 152 153 154 155 156 157 158 159 160 161 162 55 55 55
+ 55 55 55 55 55 55 55 55 55 55 55 55 55 55 55 56 56 56 56 56 56 56 56 57
+ 57 57 57 57 57 57 57 57 58 58 58 58 58 58 58 58 59 59 59 59 59 59 59 59
+ SSDC_900V_SiC_q3d2_half
.ends SSDC_900V_SiC_q3d2

.subckt SSDC_900V_SiC_q3d2_half 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22
+ 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48
+ 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74
+ 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100
+ 101 102 103 104 105 106 107 108
V1 1 109 dc 0.0
V2 2 110 dc 0.0
V3 3 111 dc 0.0
V4 4 112 dc 0.0
V5 5 113 dc 0.0
V6 6 114 dc 0.0
V7 7 115 dc 0.0
V8 8 116 dc 0.0
```

Package RLC equivalent circuit



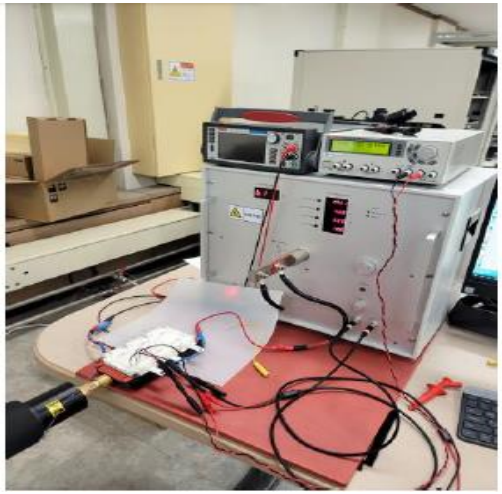
SPICE Model



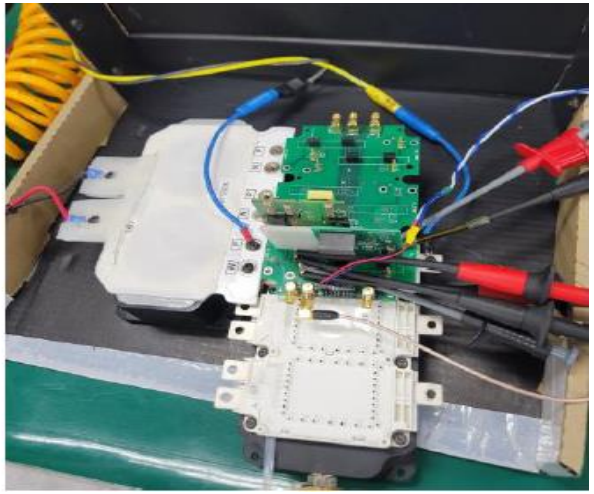
Double Pulse Simulation with Compact SPICE Model

# Simulation vs Actual test

- Important step to validate simulation accuracy
- Simulation setup needs to match actual test including: parasitics and  gate driver
- Actual samples built on typical process are characterized



DC test setup

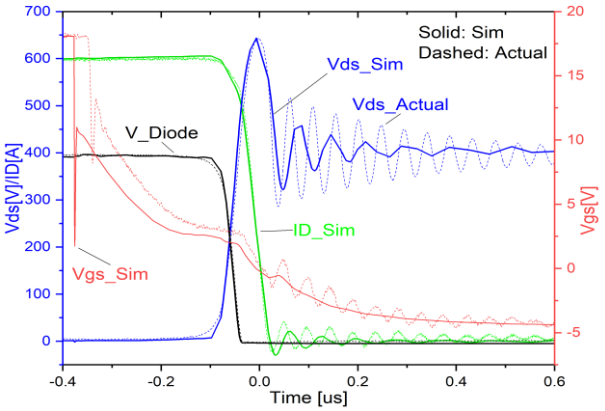


Double Pulse test setup

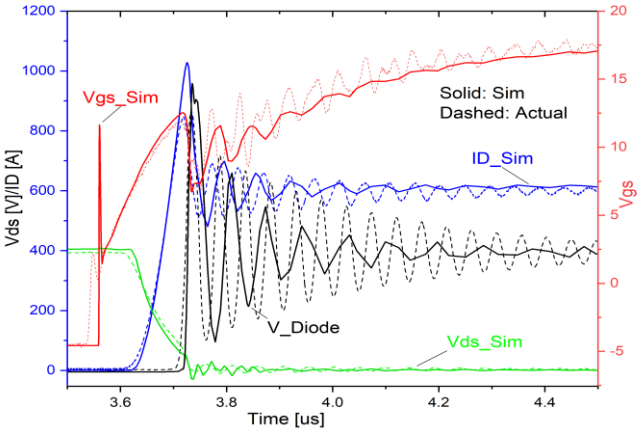

Thermal test setup

# Electrical Simulation Validation

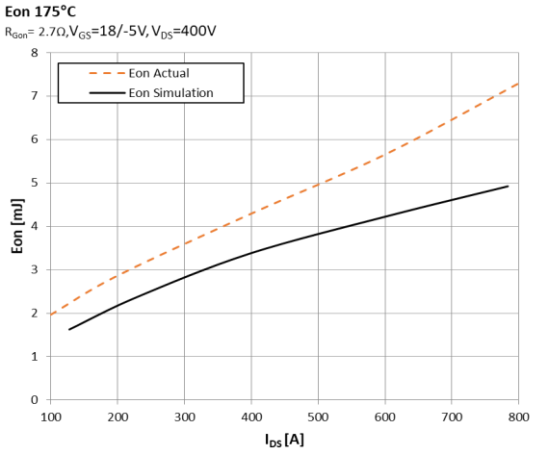
- Turning-off peak voltage, slew rate, Eoff match well
- Turning-on di/dt matches well, but voltage waveforms and Eon diverge. (further calibration ongoing)
- Modelling is validated for further die level current sharing analysis



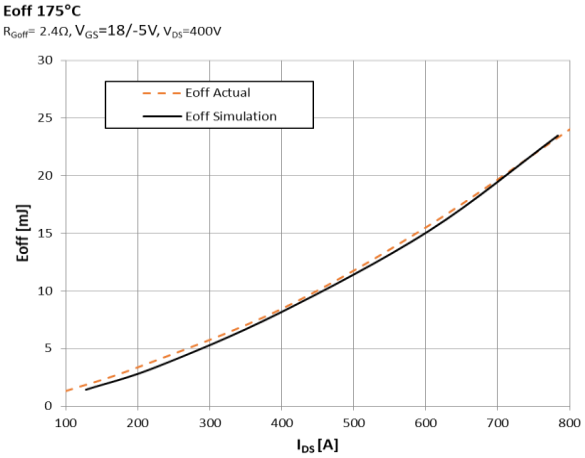

Turning-off waveforms




Turning-on waveforms



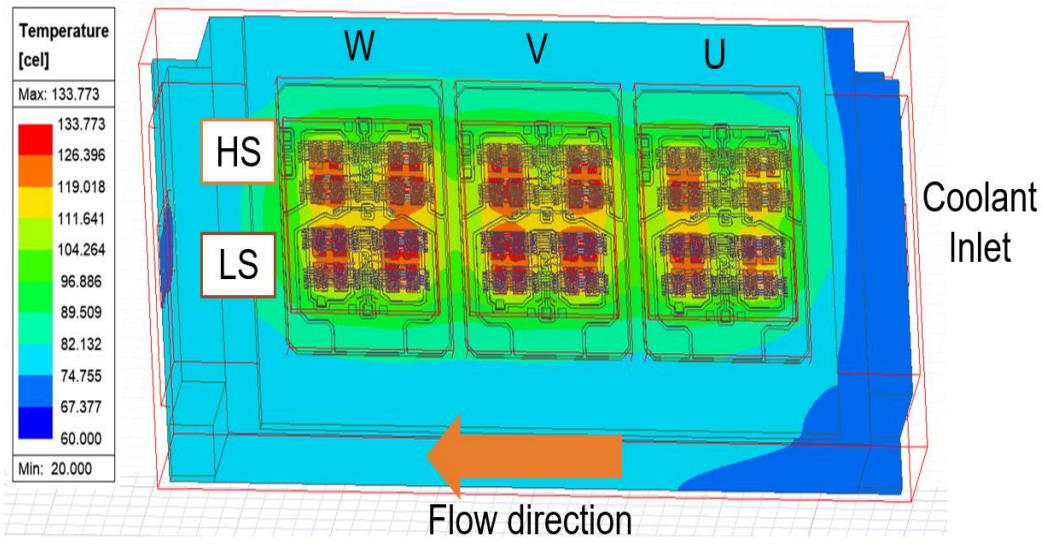

Eon vs Id



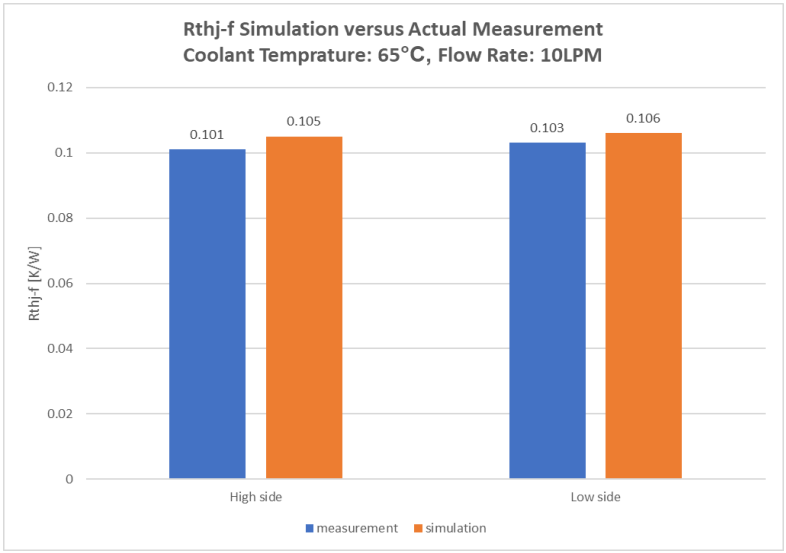

Eoff vs Id

# Thermal Simulation and validation

- Simulation vs measured, deviation within 4%
- Thermal RC network extracted with internally developed script



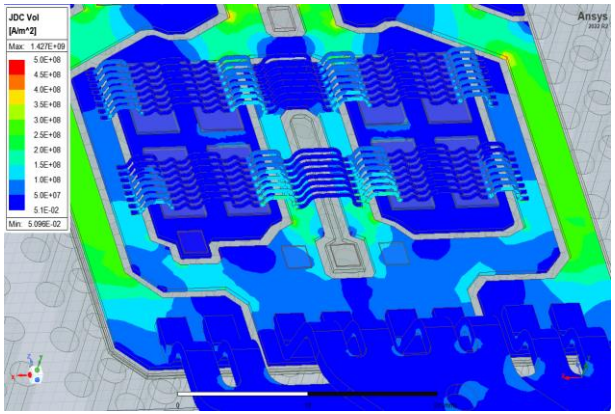

CFD simulation with Flow rate 10LPM, coolant temperature 65°C, 50W/die



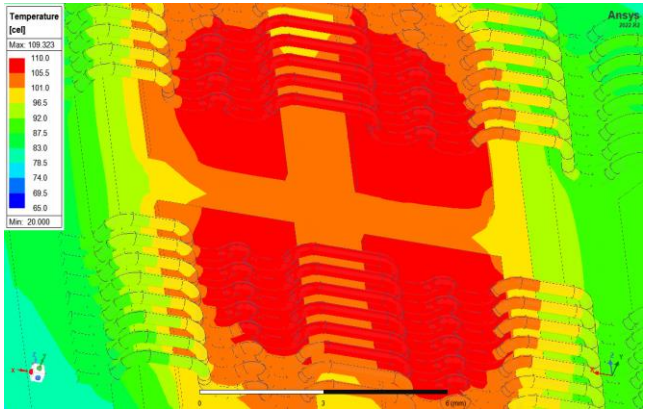

Simulation vs measured

# Joule-heating, CFD co-simulation

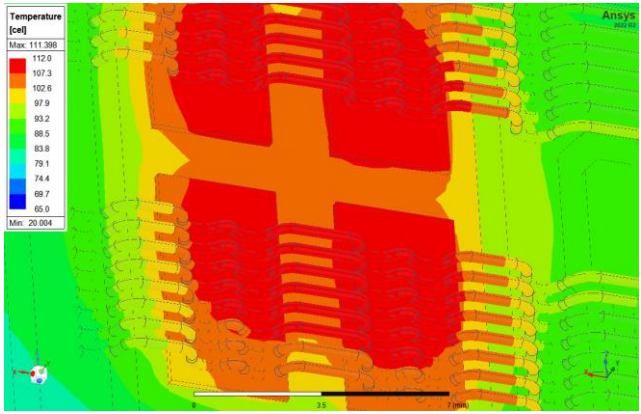
- CFD simulation coupling with EM loss from Q3D
- Slightly increased max temperature with EM loss coupled
- CFD simulation with EM loss captures temperature profile accurately




Current density profile modeled by Q3D, DC current=400A



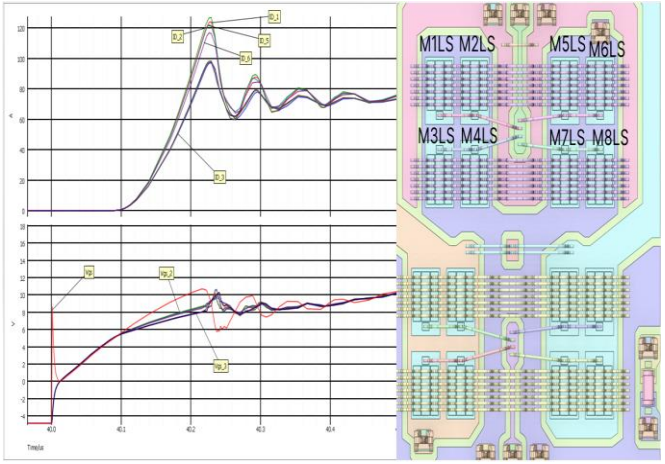

CFD simulation without EM Loss, Max temp:109C



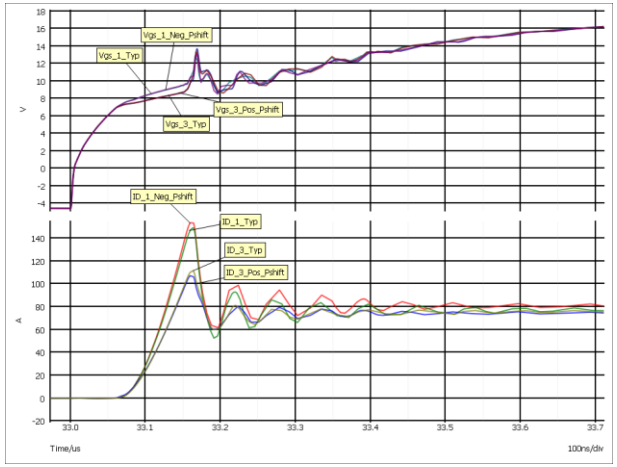

CFD simulation coupling with EM Loss, Max temp:111C

# Die level current sharing study and improvement proposal

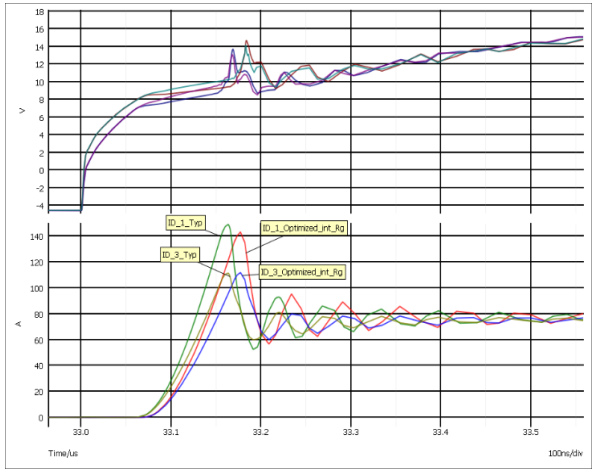
- 2 sources of mismatch are investigated: package layout and die-to-die process variation
- Each die sees different parasitic inductaces due to package layout constraints, causing current sharing mismatch
- Process variation(i.e., Rdson, Vth etc.) may further increase the mismatch
- Fine-tuning internal gate resistor is proposed to mitigate the mismatch




Package layout induced current-sharing mismatch




Die-to-die process variation induced current-sharing mismatch




Improved current-sharing with fine-tuning internal Rg

# Summary

- This paper presents a study on electrical and thermal modelling of a Silicon-Carbide power module for EV traction inverters.
- The impact of package parasitic mismatch and SiC process variation on the robustness of SiC power modules was explored.
- The work also studied the cross-coupling between Joule heating of bonding wires and power loss of SiC MOSFET die.
- The simulation results obtained demonstrated excellent alignment with actual test data.
- The research futher delved into die-level sharing to quantify current mismatch caused by package layout constraints and process variation.
- Mitigation measures are proposed to further improve the module's ruggedness.

# Thank you for the attention!

I‘m pleased to answer your questions

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